IN THE SPECIFICATION:

Please amend the specification by replacing paragraphs 1, 16, 158, 171, 207, 217, 376, 379-382, 398, 401, 404, 486, 489, 491, 493, 495, 496, 498, and 505, and adding new paragraphs 111A and 111B after paragraph 111, as shown below.

[001]   This application is a continuation-in-part of U.S. application no. ~~xx/xxx,xxx~~ 10/623,804, filed July 22, 2003, entitled "METHOD FOR OPERATING MULTIPLE OVERLAPPING WIRELESS NETWORKS" (Applicant's docket No. XSI.061), which is a continuation-in-part of U.S. application no. 10/367,834, filed February 19, 2003, entitled "M-ARY ORTHAGONAL CODED COMMUNICATIONS METHOD AND SYSTEM," which relies for priority on U.S. provisional application serial no. 60/357,638, by Matthew L. Welborn, filed February 20, 2002, entitled "M-ARY BI ORTHAGONAL CODED ULTRAWIDEBAND COMMUNICATIONS SYSTEM," U.S. provisional application serial no. 60/397,105, by Matthew L. Welborn et al., filed July 22, 2002, entitled "M-ARY BIORTHAGONAL KEY BINARY PHASE SHIFT KEY SCHEME FOR ULTRAWIDE BANDWIDTH COMMUNICATIONS USING RANDOM OVERLAY CODES AND FREQUENCY OFFSET FOR PICONET SEPARATION," U.S. provisional application serial no. 60/397,104, by Richard D. Roberts, filed July 22, 2002, entitled "METHOD AND APPARATUS FOR CARRIER DETECTION FOR CODE DIVISION MULTIPLE ACCESS ULTRAWIDE BANDWIDTH COMMUNICATIONS," and U.S. provisional application serial no. 60/398,596, by Richard D. Roberts, filed July 26, 2002, entitled "METHOD AND SYSTEM OF ACQUIRING A BINARY PHASE SHIFT KEY ULTRAWIDE BANDWIDTH SIGNAL," the contents of all of which are hereby incorporated by reference in their entirety. This application also relies for priority on U.S. provisional application serial

no. 60/ 415,527, by Richard D. Roberts, filed October 3, 2002, entitled "SYSTEM AND

METHOD OF FAST BINARY PHASE SHIFT KEY ACQUISITION," the contents of which

is hereby incorporated by reference in its entirety.

[016]   For UWB signals, robustness to multipath fading is a result not just of the wide

system bandwidth, however, but is also a result of the large ratio of system bandwidth to

center frequency, i.e., the *fractional bandwidth*. A large fractional bandwidth means that there

is a corresponding large variation in the mode and degree of RF energy interaction with the

surrounding environment over the entire UWB bandwidth. Environmental interactions such

as scattering, refraction and reflection depend on the wavelength of the RF signals, and so the

large fractional bandwidth leads to relatively low correlation in the fading properties of the

different regions of the UWB bandwidth. Thus, the properties of UWB signals should lead to

more robust multipath performance even than systems with *equal* bandwidth but much higher

center frequencies (*i.e.* lower fractional bandwidths). A more detailed analysis of this effect is

presented in a companion paper in this same issue.

[0111A]   Fig. 13 is a graph of a UWB PSD using a notch according to a preferred

embodiment of the present invention;

[0111B]   Fig. 14 is a graph of a UWB transmission scheme using two bands according to a

preferred embodiment of the present invention;

[0158]   In addition, Although Fig. although Fig. 8 shows a code word having five pulses

for the sake of simplicity, this number can be varied as needed. In fact, as noted above, 13 or

24 are preferred numbers of pulses per code word. Alternate embodiments can use any code

word length that allows system requirements to be met. For example, as clock speeds

increase, the number of pulses that can be sent in a given time will increase and longer code

word lengths may be used.

[0171]   In alternate embodiments, an oscillating signal could be further modulated by a

carrier signal having a lower frequency (e.g., 1/N). In this case, the carrier could serve to

modulate a set of N repetitions of the oscillating signal. These N repetitions of the oscillating

signal (modulated by the carrier) form a pulse. This is similar to the embodiment of Fig. 9A,

with the addition of the carrier signal.

[0207]   By having the high and low bands located where they are, and of the width they are,

the UWB transmission system shown in Fig.14 limits its interference with any other signals

being transmitted in the UNII band, while also providing two separate transmission paths.

[0217]   The lookup table 1530 receives a bit stream, breaks the bit stream up into n-bit

groups, and determines the proper code word associated with that particular n-bit group. It

then sequentially outputs a series of "1"s and "0"s corresponding to the proper code word. In

this embodiment n can be any integer greater than 0. Although this preferred embodiment

uses a lookup table 1530, alternate embodiments could use other circuitry to perform this

same function.

[0376]   The system then adds, using complex math notation, the difference between the

squared unsynchronized in-phase component and the squared quadrature phase component

with twice the product of the unsynchronized in-phase component and the quadrature phase

component to obtain a CCA input value $\sout{[I^2 - Q^2 + 2(I \times Q)]}$ $[I^2 - Q^2 + j2(I \times Q)]$. (Step 2107)

[0379] Although Figs. 21A and 21C show one way of calculating the quantity

~~$[I^2 - Q^2 + 2(I \times Q)]$~~ $[I^2 - Q^2 + j2(I \times Q)]$, alternate methods and circuits are possible using

different arrangements of circuitry, and performing operations in different orders.

[0380] As shown in Fig. 21B, the clear channel assessment circuit 2100b includes an

antenna 2110, an RF front end 2115, a first mixer 2120, a second mixer 2125, a base

oscillator 2130, a first 0/90 phase shifter 2135, a loop filter 2132, a voltage-controlled

oscillator (VCO) 2134, a second 0/90 phase shifter 2136, a first low pass filter (LPF) 2140, a

second LPF 2145, a first squaring circuit 2150, a second squaring circuit 2155, an adder

2160, an inverting buffer 2165, a third mixer 2170, a fourth mixer 2172, a fifth mixer 2174, a

doubling buffer 2175, <u>an absolute value circuit 2182,</u> an automatic gain control (AGC) loop

filter ~~2180~~ <u>2184</u>, and a decimated fast Fourier transform (FFT) 2185. Elements in Fig. 21B

that have the same reference numbers as in Fig. 21A operate in a similar manner.

[0381] Although this circuit may be performed entirely using analog circuitry in some

embodiments, in a preferred embodiment analog-to-digital converter (ADCs) can be used at

some point along the signal stream to perform part of the operation digitally. In a preferred

embodiment, a first ADC 2190 is placed between the first LPF 2140 and the first squaring

circuit ~~2150~~ <u>2172</u>, and a second ADC 2195 is placed between the second LPF 2145 and the

second squaring circuit ~~2155~~ <u>2174</u>. However, in alternate embodiments, the number and

placement ADCs could be altered, or they could be eliminated altogether.

[0382] In operation, the clear channel assessment circuit ~~2190b~~ <u>2100b</u> operates as follows.

A signal comes in at the antenna 2110. This signal is sent through the front end 2115, which

preferably includes a variable gain amplifier controlled by feedback from the AGC loop filter

2180. Once the incoming signal has been processed through the front end 2115, it is provided

to inputs in both the first and second mixers 2120 and 2125. These two mixers 2120 and

2125 mark the beginning of what can be called I and Q paths for the incoming signal, and this

process of breaking the signal up into I and Q paths can be called I/Q demodulation.

[0398]   As noted above, one way to look at the clear channel assessment circuit ~~2100a~~

2100b is to consider that it breaks the incoming signal into a real portion x output from the

first LPF 2140, and an imaginary portion y output from the second LPF 2145. And based on

Equation (18), the output of the adder 2160 represents the real portion of the square of the

input signal, while the output of the doubling buffer represents the imaginary portion of the

input signal.

[0401]   The ACG loop filter 2180 is preferably a first order control loop filter with an

output proportional to the error signal at the input. Other filters are possible, however, in

alternate embodiments. The ACG loop filter 2184 filters the output of the absolute value

circuit 2182 and provides the result to the front end ~~2120~~ 2110 as a feedback signal.

[0404]   In a preferred embodiment, the clear channel assessment circuit ~~2100a~~ 2100b

operates with analog circuitry up until the first and second LPFs ~~2130 and 2135~~ 2140 and

2145, and operates with digital circuitry thereafter. Therefore, in this embodiment the first

ADC 2190 is inserted between the first LPF 2130 and the first squaring circuit ~~2140~~ 2172,

and the second ADC 2195 is inserted between the second LPF 2135 and the second squaring

circuit ~~2145~~ 2174. In alternate embodiments the analog/digital line could be moved, or the

whole operation could be performed in the analog realm.

[0486]   As shown in Fig. 22B, a normal preamble 2202 includes an AGC/CCA portion

2210, a normal synchronization portion 2222, a normal decision feedback equalization (DFE)

training portion 2250 2252, an SFD 2230, and a PHY header 2240.

[0489]   The normal DFE training portion 2250 2252 provides time and information for the

receiver to perform decision feedback equalization on the incoming signal. In the preferred

embodiment disclosed in Fig. 22B, the DFE training portion 2250 is 4 µs long.

[0491]   The PHY header 2250 2240 provides time and information to allow the receiving

device to perform what acquisition operations are necessary based on the particular PHY

layer being used. The specific parameters of the PHY header 2250 2240 will vary as different

PHY layers are used.

[0493]   As shown in Fig. 22C, a long preamble 2203 includes an AGC/CCA portion 2210,

a long synchronization portion 2223, a DFE training portion 2250 2253, an SFD 2230, and a

PHY header 2240.

[0495]   The long synchronization portion 2223 provides the receiver with a known set of

data that allows the receiving device to lock onto the chipping clock and the symbol clock of

the transmitter. In other words, it allows the receiver to synchronize with the phase of the

pulses being transmitted as well as the phase of the symbols being transmitted. In the

preferred embodiment disclosed in Fig. 22C, the chip and symbol clock lock synchronization

portion 2222 2223 is 91.5 µs long.

[0496] The DFE training portion ~~2260~~ 2253 provides time and information for the receiver to perform decision feedback equalization on the incoming signal. In the preferred embodiment disclosed in Fig. 22C, the DFE training portion 2260 is 4 μs long.

[0498] The PHY header ~~2250~~ 2240 provides time and information to allow the receiving device to perform what acquisition operations are necessary based on the particular PHY layer being used. The specific parameters of the PHY header ~~2250~~ 2240 will vary as different PHY layers are used.

[0505] For example, if after a time the data signal was found to be very strong, the network might move from the normal preamble 2202 to the short preamble 2201 in order to increase data transmission rate. Then, if for some reason the signal strength degrades and acquisition becomes harder, the network can return to the normal preamble ~~220~~ 2202, or even move to the long preamble 2203.